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L18	1	("6646397").PN.	US-PGPUB; USPAT	OR	OFF	2005/01/31 12:02
L19	139	hardware-in-the-loop	US-PGPUB; USPAT	OR	ON	2005/01/31 12:02
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[Abstract] [PDF Full-Text (180 KB)] IEEE JNL

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Kang-Ngee Chia; Hea Joung Kim; Lansing, S.; Mangione-Smith, W.H.; Villasensor, J.;
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Welch, J.T.;
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McKenzie, N.R.; Ebeling, C.; McMurchie, L.; Borriello, G.;
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Babb, J.; Tessier, R.; Dahl, M.; Hanono, S.Z.; Hoki, D.M.; Agarwal, A.;
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Chung, J.W.; Kim, J.S.; Jeong, Y.G.; Ha, J.S.;
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The Chinook Hardware/Software Co-Synthesis System - Chou, Ortega, Borriello (1995) (Correct) (18 citations)
circuits including **microprocessors**, **programmable logic**, and devices such as LCDs, network **processors** and/or custom logic and the co-**simulation** of system specifications before, during, and are applied to a window of data samples. Digital **signal** processing (DSP) systems are the canonical
ftp.cs.washington.edu/tr/1995/03/UW-CSE-95-03-04.PS.Z

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Run-Time Compaction of FPGA Designs - Diessel, ElGindy (1997) (Correct) (11 citations)
Y. K. Cheung, and M. Glesner, editors, Field-**Programmable Logic** and Applications, 7th International bit-streams with new offsets. We show by **simulation** that significant performance improvements are at least one order of magnitude greater than the **signal** delay of a cell or the latency of a wire. We
ftp.cs.newcastle.edu.au/pub/techreports/tr97-02.ps.Z

A Compiler for Application-Specific Signal Processors - Rimey, Hilfinger (1988) (Correct) (10 citations)
it is actually a state machine based on a **programmable logic** array, it can simultaneously evaluate any not strictly compatible with C. For behavioral **simulation**, we provide a translator that converts RL into A Compiler for Application-Specific **Signal Processors** Ken Rimey and Paul N. Hilfinger
www.cs.hut.fi/~rimey/papers/monterey/paper.ps

Increasing Microprocessor Performance with.. - Sawitzki, Gratz, Spallek (1998) (Correct) (8 citations)
microprocessor cores with tightly-coupled **programmable logic** started to appear [7-9]In this paper we and reconfigurable logic on the same die. **Simulations** have shown that even a comparatively simple be easily scaled. The **simulation** of the critical **signal** path within CoMPARE indicates that the 8-bit
www.inf.tu-dresden.de/~ss9/fpl98.ps.gz

Cameron: High Level Language Compilation for.. - Hammes, Rinker.. (1999) (Correct) (7 citations)
based on FPGAs, which are large arrays of **programmable logic** cells, organized into one or more arrays of code and FPGA configurations. The compilation, **simulation** and execution path, shown in figure 1, uses and Hutchings specifically consider digital **signal** processing tasks, and also calculate a ten-fold
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ASOC: A Scalable, Single-Chip Communications Architecture - Liang, Swaminathan, Tessier (2000) (Correct) (2 citations)
Corporation, integrates a microcontroller, **programmable logic**, and a number of peripherals (UART, SoC interconnect architectures via parallel **simulation**. Additionally, a preliminary layout of our attributed to two factors: capacitive off-chip **signal** delays and a need for growing numbers of
www.ecs.umass.edu/ece/tessier/courses/669/pact00.ps.gz

A Framework for Developing Parametrised FPGA Libraries - Luk Guo (1996) (Correct) (2 citations)
FastMap **processor** interface"in Field **Programmable Logic** and Applications, W. Moore and W. Luk Third, while some library generators provide **simulation** models for their circuits, there is no and adders increasingly complex libraries for **signal** processing and other applications are beginning
www.doc.ic.ac.uk/~wl/papers/fpl96.ps.gz

Simulation of Evolvable Hardware to Solve Low Level.. - Hollingworth.. (1999) (Correct) (1 citation)
Gate Array (FPGA)7] devices and **Programmable Logic** Devices (PLD)since these can be **Simulation** of Evolvable Hardware to Solve Low Level Image
filter, which is simple to implement on Digital **Signal Processor**(DSP) technology. The first step in
www.amp.york.ac.uk/external/media/cal/bio-insp/publications/gsh-evoiasp99.pdf

Using Large CPLDs and FPGAs for Prototyping and VGA Video.. - James Hamblen School (1999) (Correct) (1 citation)
tools and higher gate capacity CPLD, Complex **Programmable Logic** Device, and FPGA, Field Programmable Gate

to provide students with logic synthesis and **simulation** CAD tools and to provide low cost hardware using hardware inside the CPLD or FPGA. Only five **signals** or pins are required, two sync **signals** and www.ece.gatech.edu/users/hamblen/ALTERA/wcae98.PDF

An Array Architecture for Reconfigurable Datapaths - Wang, Gulak (1993) (Correct) (1 citation)
C =Carry Logic Block L L L Table Lookup **Programmable Logic** Box Programmable Routing Box Programmable examples are presented. The design modelling and **simulation** of the datapath using VHDL are described and we for a simple routing interconnection for control **signals**. Other features can be exploited in the design www.eecg.toronto.edu/~qiang/research/papers/paperOxford.ps

An Array Architecture for Reconfigurable Datapath - Wang (1998) (Correct) (1 citation)
Logic Block L L L Table Lookup Invertor **Programmable Logic** Box (a) The Programmble Routing and Logic sequence is used as a test vehicle in the **simulations**. Qiang Wang An Array Architecture for FPGAs to prototype **microprocessors** and digital **signal processors** of various types. An FPGA consists of www.eecg.toronto.edu/~qiang/research/theses/Mthesis.ps

The CPU Design Kit: An Instructional Prototyping Platform for.. - Anujan Varma (1995) (Correct) (1 citation)
be explored. With the availability of dense **programmable logic** chips such as the Altera FLEX series, it environment for design entry, synthesis, and **simulation** of the system from a high-level language the register file and caches, monitor the state of **signals** on the board, and control execution of the CPU. ftp.cse.ucsc.edu/pub/hsnlab/cpukit.ps.Z

Resume - Panchal (Correct)
Programming, testing and installation of **programmable logic** controllers (GE-Fanuc)B.E. Thesis work : A Methodology of Modeling Wireless Networks **Simulation** Advisors: Prof. Roy Yates and Prof. Andrew (B.E. thesis) The project is based on digital **signal** processing and artificial neural networks. www.caip.rutgers.edu/~jpanchal/resume/resume.ps

Design of Highly Parallel Edge Detection Nodes Using.. - Hollingworth, Smith.. (1999) (Correct)
gap to engineering, but with the advent of **programmable logic** devices, such as FPGAs, the interest of to the particular images encountered. The **simulation** of such a system through the use of be simple to implement (particularly on Digital **Signal Processor** (DSP) technology) and are particularly www.amp.york.ac.uk/external/media/cal/bio-insp/publications/gsh-pdp99.pdf

Unknown - (Correct)
main categories of FPDs: simple and complex **programmable logic** devices, and field-programmable gate Using Vhdl For Board Level **Simulation** Sandi Habinc European Space Agency Peter estimating transition probabilities of internal **signals** in combinational circuits uses Markov chains and www.iro.umontreal.ca/~aboulham/synthA97.pdf

A Concept for an Evaluation Framework for Reconfigurable Systems - Sawitzki, Spallek (1999) (Correct)
as a combination of hardwired and **programmable logic**. The coupling between these components is in the time-consuming development of dedicated **simulation** and prototyping environments, especially if the [8]A benchmark set consisting of three digital **signal** processing algorithms was run on a variety of www.inf.tu-dresden.de/~ss9/fpl99.ps.gz

High--Bandwidth Trace Collection for Multicomputer.. - Charles Hudnall (Correct)
probes to memory is implemented in **programmable logic**. Breakpoint-style debugging support is Research Center for Computational Field **Simulation** Mississippi State University Abstract is also provided via the SPInet Halt/Resume **signals**. The design of the SPIcontrol board is driven by www.erc.msstate.edu/thrusts/ca/html/../publications/SSSTSPIcontrol.ps.gz

Finite-Word-Length and Nonrecursive Implementation of.. - Fischer, Huber (1997) (Correct)
processor, but it is necessary to employ **programmable logic** devices (PLDs) or application specific input is described analytically. Examples and **simulation** results demonstrate the validity of these interest. Because, over the last decade, digital **signal** processing has made a big progress, high-rate www-nt.e-technik.uni-erlangen.de/~dcg/papers/aeu_97.ps.gz

Application of a TMS320C31 chip for DSP/Embedded System - Feng, Olsen, Pietraski.. (Correct)
In addition, the system has several **programmable logic** devices[5] to program the counting function facilitate computer **simulation**, debugging and embedded-system development. To

development on a fixed platform. TMS320C31 read **signal** write **signal** Active Buffer Pod SN74ACT8990 Test
adwww.fnal.gov/www/icalepcs/abstracts/Postscript/fpo46.ps

Flexible codesign target architecture for early.. - Tammemäe, O'Nils, Hemani (Correct)
of System Synthesis, ISSS'95. 12. The **Programmable Logic** Data Book"Xilinx, Inc.1994. 13. M.
from HW side, thus establishing real clock-level **simulation**. Coemulation. Hardware is programmed into FPGA
initialises selected function. After completion **signal** "done" can be polled out from server (HW) status
www.ele.kth.se/ESD/doc/ar96/nalle/springer.ps.gz

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with real-time issues, human-in-the-**loop** or **hardware**-in-the-**loop**. Whether a **simulation** is discrete
been concerned with real-time issues, human-in-the-**loop** or **hardware**-in-the-**loop**. Whether a **simulation** is
A Spectrum Of Options For Parallel **Simulation** Paul F. Reynolds, Jr. Ipc-Tr-88-007 Sept. 9,
ftp.cs.virginia.edu/pub/techreports/IPC-88-07.ps.Z

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SPECTRUM: A Parallel Simulation Testbed+ - Reynolds, Jr., Dickens (1989) (Correct) (5 citations)
with real-time issues, human-in-the-**loop** or **hardware**-in-the-**loop**. In [Reyn88] we showed that,
been concerned with real-time issues, human-in-the-**loop** or **hardware**-in-the-**loop**. In [Reyn88] we showed
Spectrum: A Parallel **Simulation** Testbed Paul F. Reynolds, Jr. Phillip M.
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Modeling And Realtime Simulation Of An Automatic Gearbox .. - Otter, Schlegel.. (1997) (Correct) (3 citations)
object oriented modeling, automatic gearbox, **hardware**-in-the-**loop simulation**, Modelica. ABSTRACT To
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Modeling And Realtime **Simulation** Of An Automatic Gearbox Using Modelica Martin
www.op.dlr.de/FF-DR/dr_er/staff/otter/../../publications/1997/otter_ess.ps.gz

A Step towards Operating System Synthesis - Ditze (1998) (Correct) (1 citation)
when considering design methodologies like **Hardware**-in-the-**Loop**: Starting with a pure (distributed)
embedded subsystems. Usually, a high-level control **loop** executes a large block of software instructions at
Starting With A Pure (distributed) **Simulation** The Entire System Requires A Distributed Hpc Os
www.uni-paderborn.de/sfb376/projects/b1/PS/Dit98a.ps.gz

Bruce E. Tucker - Kenneth Zabel Sparta (Correct)
by this computation is used as part of a **hardware**-in-the-**loop** (HWIL) RTTC test facility, which
computation is used as part of a **hardware**-in-the-**loop** (HWIL) RTTC test facility, which tests imaging
for a real-time **hardware**-in-the-**loop** (HWIL) **simulation** facility at the U.S. Army Redstone Technical
fly.hiwaay.net/~betucker/itea_paper.pdf

Modeling Of Hydraulic Systems For Hardware-In-The-Loop.. - Ferreira, al. (Correct)
Modeling Of Hydraulic Systems For **Hardware**-In-The-**Loop Simulation**: A Methodology Proposal
Modeling Of Hydraulic Systems For **Hardware**-In-The-**Loop Simulation**: A Methodology Proposal Jorge A.
Of Hydraulic Systems For **Hardware**-In-The-**Loop Simulation**: A Methodology Proposal Jorge A. Ferreira
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Comparative analysis between automatic design methodology and.. - Cilio (1996) (Correct)
. 10 2.1.3 **Hardware** subsystem .
cardit.et.tudelft.nl/MOVE/papers/cilio96.ps.gz

Real Time Simulation and Online Control for.. - Chucholowski.. (1999) (Correct)
must be performed in real time for application in **Hardware**-in-the-**Loop** experiments. Numerical results are
in real time for application in **Hardware**-in-the-**Loop** experiments. Numerical results are presented for
Real Time **Simulation** and Online Control for Virtual Test Drives of
www-m2.mathematik.tu-muenchen.de/~stryk/paper/1998-fortwihr-tesis.ps.gz

Hardware/software Co-Design For Dsp Applications Via The Hms.. - Michael Sheliga (Correct)
Hardware/software Co-Design For Dsp Applications Via The
algorithms for performing partitioning, scheduling, **loop** pipelining (retiming)**hardware** needability
the least design time. They also require less **simulation**, test and verification time. However,

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